A Cross-Coupled LC Voltage-Controlled Oscillator with Varactor Tuning and Digital Band Switches in 45-nm CMOS

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Academic Integrity Statement

I certify that this report represents my original work. No prior-year designs, reports, or external unpublished materials were used. All assistance from tools such as AI is disclosed where applicable.

Contents

Abbreviations List

Acronym	**Definition**
AC	Alternating Current
ASITIC	Analysis of Si Inductors and Transformers for ICs
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
dB	Decibel
DC	Direct Current
GND	Electrical Ground
IC	Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-Channel Metal-Oxide-Semiconductor
PLL	Phase-Locked-Loop
PVT	Process, Voltage, and Temperature
VCO	Voltage-Controlled Oscillator
VDD	Positive Supply Voltage

1 Abstract

The presented LC cross-coupled NMOS VCO was designed using a high-Q differential ASITIC inductor, an analog frequency tuning varactor, a bias resistor, and discrete frequency band selection bits. The digital capacitor switches were included to divide the tuning range into four overlapping bands and designed to have roughly equivalent Q by halving the switch resistance, doubling the transistor width, and doubling the capacitance for each successive bit. An analog varactor was then used for fine frequency control within each band. The VCO achieved a monotonic tuning range of 6.61–7.37 GHz. The phase noise remained below -114 dBc/Hz at a 1 MHz offset, the power consumption was 1.93 mW, the maximum VCO gain was less than 493 MHz/V, and the differential output swing was 1.13 $\mathrm{V_{ppd}}$. The two digital capacitor bits created an average band overlap of approximately 30%.

2 Specifications Table

Summary of performance versus required specifications. Specifications not met appear in red.

Metric	**VCO Specification**	**Achieved Value**	**Meets Spec?**
Tuning Range	6.7–7.3 GHz, monotonic	6.61–7.37 GHz	Yes
Phase Noise	< -110 dBc/Hz at 1 MHz offset	< -114 dBc/Hz at 1 MHz offset	Yes
Power Metric	$\mathrm{P_{dc}} < 20\,\mathrm{mW}$	1.93 mW	Yes
VCO Gain	$K_{\mathrm{VCO}} < 500\,\mathrm{MHz/V}$	$< 493\,\mathrm{MHz/V}$	Yes
Differential Output Swing	$V_{\mathrm{swing}} > 1.0\,\mathrm{V_{ppd}}$	$> 1.13\,\mathrm{V_{ppd}}$	Yes

Table 1: VCO design specifications and achieved simulated performance.

3 Use of AI Tools

OpenAI's ChatGPT 5.4 Model was used for textual grammar edits, help with LaTeX formatting, and revisions for clarity in the report.

4 Technical Discussion

4.1 Design Overview

The oscillator is a fundamental building block in RF transmitters and receivers. It provides a local oscillator signal for phase-locked loop circuitry, synthesizers, mixers, etc. As such, a VCO must provide accurate and stable frequencies, low phase noise, a sufficient tuning range, a linear tuning response, low power consumption, a small footprint, and robustness to Power-Voltage-Temperature (PVT) variation to ensure coherent/reliable communication systems.

This project uses a fully differential LC cross-coupled VCO architecture as it oscillates easily, provides a differential output, and good phase noise performance. In this topology, the LC tank resonance sets the oscillation frequency, with a finite-Q loss, while the cross-coupled NMOS pair (essentially diode-connected devices with inversions in their loop) provide a negative resistance (tuned with gm by adjusting tail current) to counteract the LC loss. The magnitude of the negative conductance cell must be larger than the positive loss conductance of the LC tank to sustain oscillation. This results in an oscillation whose amplitude grows until it is limited by device nonlinearities and or voltage/current saturation. It is interesting that the positive feedback effectively filters the signal with a band pass response at each stage (similar to linewidth narrowing), which results in a sharp delta-like frequency spectrum at resonance (affected by Q-factor of the resonator).

The resonant tank includes a differential ASITIC inductor, which improves the Q as it increases the substrate parasitic impedance. To generate capacitive reactance, NMOS inversion-mode varactors are used for analog tuning and digital switch-capacitor banks are used for course tuning. The varactor control voltage is ideally set by a negative feedback mechanism from a PLL while the switch-capacitor banks divide the total frequency range into multiple overlapping bands. It is important to note that this reduces the required analog varactor range for tuning, which subsequently lowers K_{VCO}, reduces phase-noise, and prevents the VCO gain from collapsing. For the digital switched-capacitors, an inverter was not used as there was no limit digital control voltages for the project. Additionally, each capacitor bit was designed to have roughly equivalent Q (the capacitance was doubled and the effective series resistance was halved for each successive binary-weighted bit).

In terms of noise, a simple tail resistor was used as a current source, instead of an active current mirror, to reduce flicker noise being unconverted, or mixed, from the bias circuitry. Additionally, noise of phase-type, rather than amplitude, is dominant in a VCO and under inspection for this report as the oscillator amplitude is limited by the large-signal nonlinearities of the cross-coupled pair.

***Note all information here was sourced from Dr. Floyd's Lectures.

4.2 Design Methodology

The VCO was designed with a simple NMOS-only cross-coupled topology. This was selected as the positive-feedback g_m cell as it can result in a high f_T (ratio of g_m to fixed capacitance).

Step 1: In a single-transistor NMOS test bench, sweep V_{GS}, number of fingers, and examine g_m current and total capacitance to determine device size.

Step 2: Build an ideal LC cross-coupled VCO core with NMOS devices, an inductor with $Q \approx 10$, an ideal capacitor, and a tail current source. Add an initial-condition startup aid and set $V_{\text{out}+} = 1$ V and $V_{\text{out}-} = 0.99$ V (this breaks the symmetry).

Step 3: Add dummy NMOS buffer loads. Connect the the source/body/drain so that it represents the input capacitance of a following NMOS buffer.

Step 4: Determine $LC_{\max}$ (minimum frequency) and $LC_{\min}$ (maximum frequency). Choose a smaller L, since it allows for more variable capacitance in the tank. However, a smaller L results in a smaller tank resistance, meaning higher transistor g_m is needed for a given loop gain, which increases power but can improve phase noise.

Step 5: Sweep L_{tank}. Leave a placeholder for a fixed capacitance and chose a moderate inductor value of < 1 nH.

Step 5: Design *symsq* inductor. Keep width moderate and spacing small to achieve $Q > 12$.

Step 6: Sweep fixed tank capacitance and decide on $C_{\min}$ and $C_{\max}$. Split the tuning range into four bands. Calculate the slope for the VCO gain and size the varactor and digital switches so that there is an ideal 40% overlap. Add fixed *mimcap* to offset tuning range to 7GHz . Use ideal analogLib capacitors to verify math and tuning ranges.

Step 7: Switch to using a tail resistor such that the core current is set by the common-mode tail voltage instead of a current source. Increase resistor value if phase noise is too high.

Step 8: Build the digital switches while keeping the ideal varactor. Size such that each capacitor bit has roughly equivalent Q (capacitance doubles and the effective series resistance was halves for each successive binary-weighted bit). Use resistances $> 100\text{k}\Omega$ for the first bit.

Step 9: In varactor test bench, scale the number of fingers to achieve chosen capacitance delta. Be sure to work with the monotonic portion of the capacitance curve, so that the capacitance moves in only one direction as V_{tune} is swept.

Step 10: Finalize the design by adjusting the value of the mimcap and slightly tuning the varactor to adjust the total offset of the entire frequency range.

5 Voltage Controlled Oscillator Schematics (Design Values)

5.1 Voltage Controlled Oscillator Core

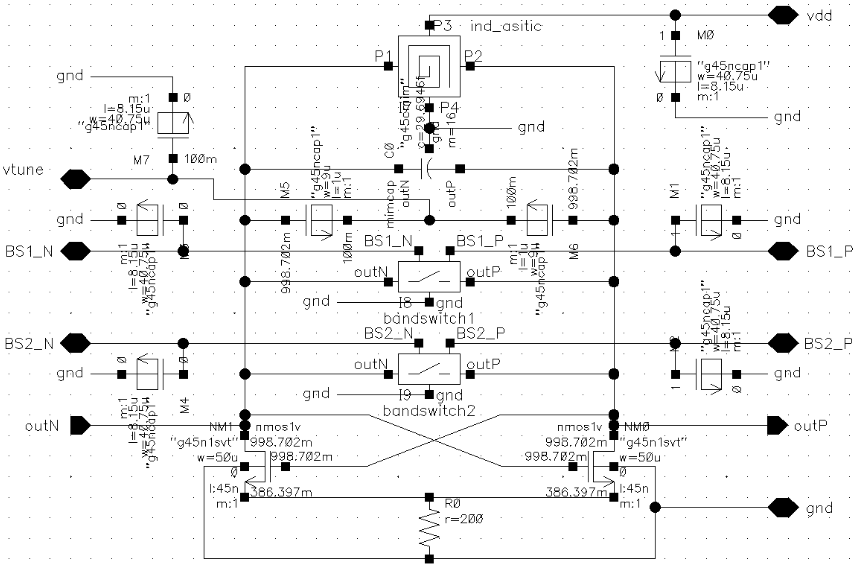


Figure 1: The VCO features an ASITIC modeled differential inductor, a NMOS cross-coupled pair, two band switches, a mimcap offset capacitor, and an analog varactor. AC decoupling capacitors are included on DC lines.

5.2 Voltage Controlled Oscillator Test Bench

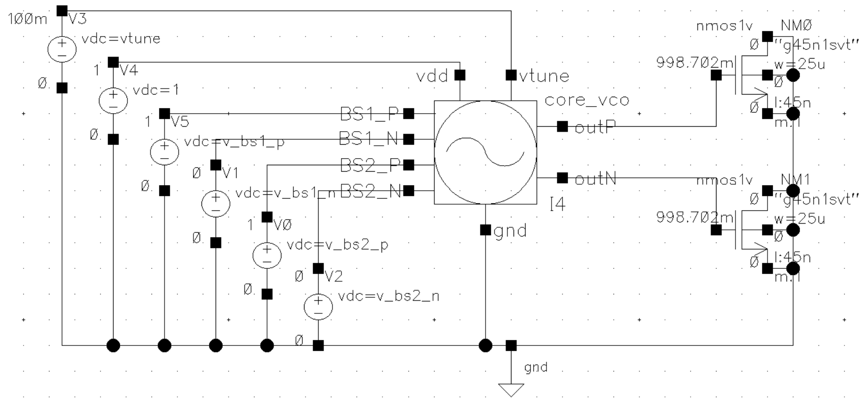
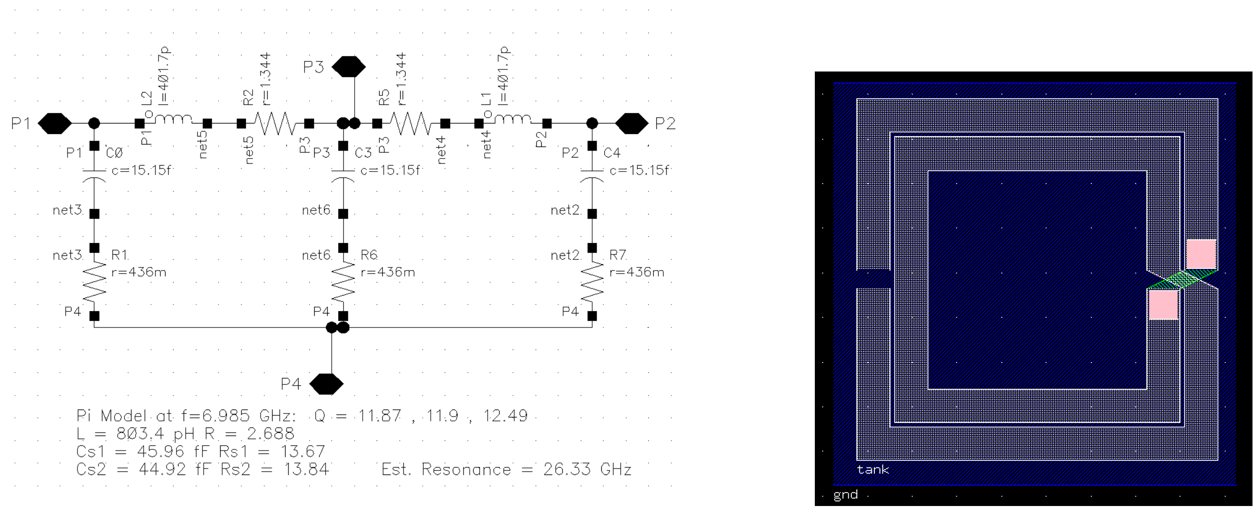


Figure 2: The VCO test bench includes four ideal digital voltage sources, a VDD source of 1V, and a VDC tuning source (meant to come from a PLL). The dummy transistor capacative loads are half the size of the core devices in the VCO.

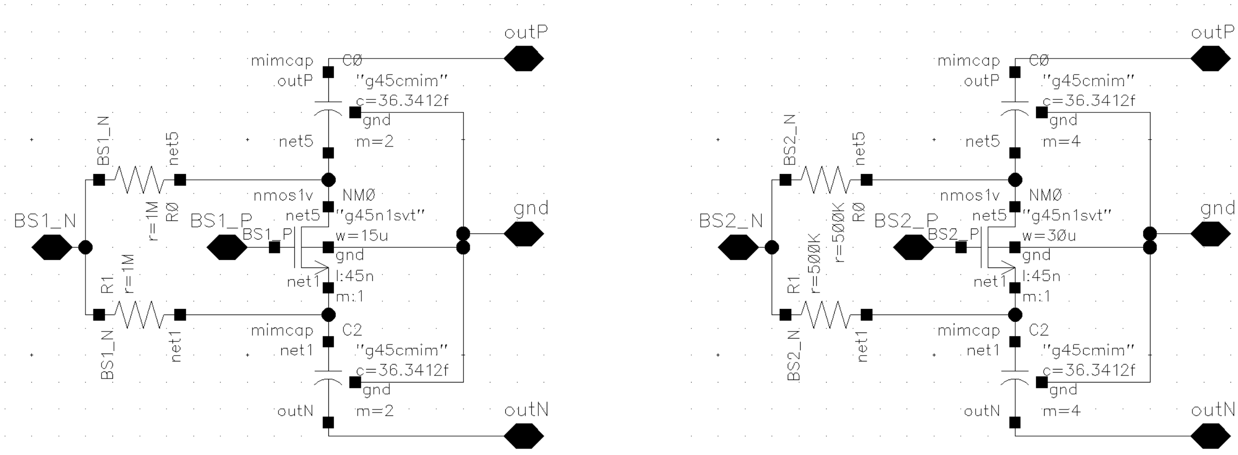
5.3 ASITIC Modeled Tank Inductor



(a) Schematic (b) Layout

Figure 3: The differential inductor ($Q = 12.49$) was modeled with an outer edge-to-edge length of 162 μm, a metal width of 15 μm, 2 μm trace spacing, 8 μm transition spacing, and two turns. The spiral was implemented on the top metal layer (M6) with an M5 transition layer. A 180 μm×180 μm ground shield was added on M1 with an electrical phase of +1 and a 0° spiral orientation to reduce parasitic capacitance between the substrate and improve the inductor Q.

5.4 Digitally Controlled Band Switches



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(a) Band Switch 1 (b) Band Switch 2

Figure 4: The digital band switches feature mimcaps, a transistor, and AC blocking resistors. The Q-factors of successive bit switches are designed to be roughly equivalent by halving the resistance, doubling the width of the transistor, and doubling the capacitance.

5.5 Analog Varactor Test Bench

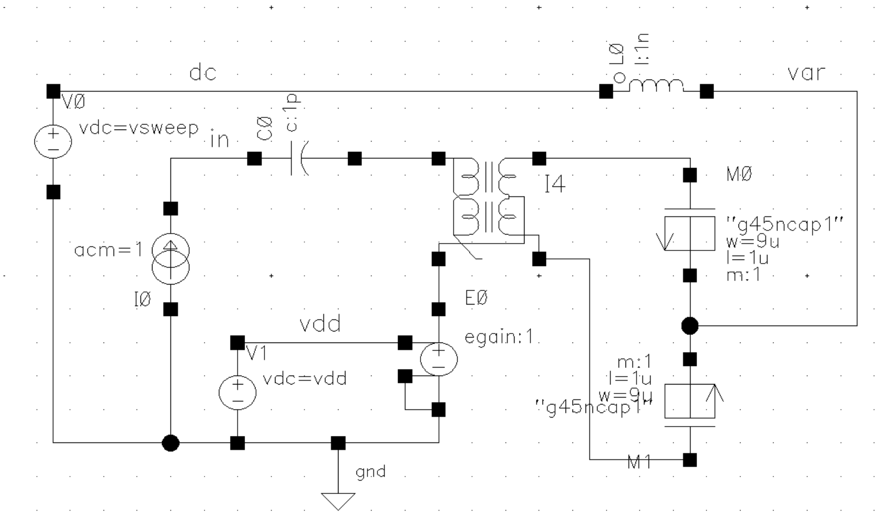


Figure 5: The analog varactor test bench utilizes an ideal balun component along with an ideal input bias T network to evaluate the capacitance across the differential varactor as tuning voltage is swept.

6 Voltage Controlled Oscillator Simulation Results

6.1 Varactor Capacitance and Quality Factor vs. Control Voltage

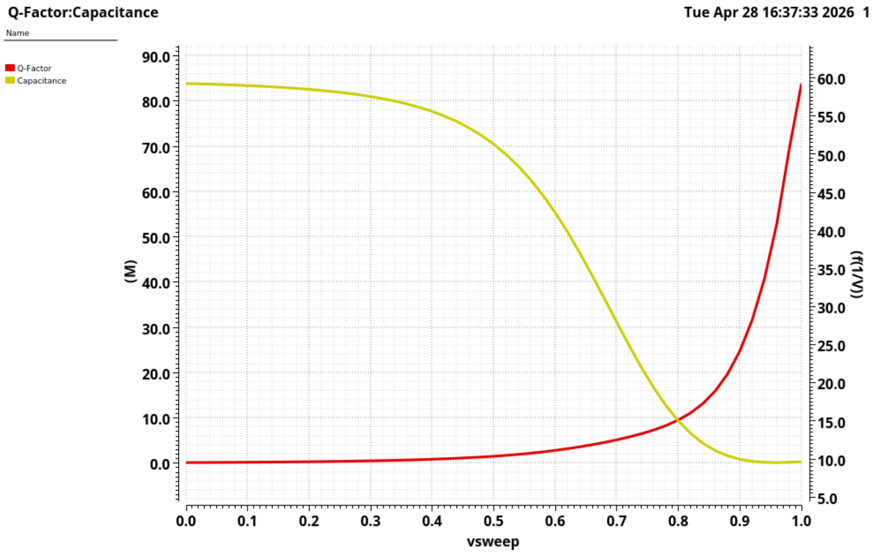


Figure 6: Simulated varactor capacitance and quality factor versus V_{tune}. The capacitance is monotonic over the selected 0.1–0.9 V tuning range, although a more linear region would be preferred. The extracted Q is unrealistically high due to low series resistance.

6.2 Transient Response at the Low, Mid, and High-Frequency Tuning Points

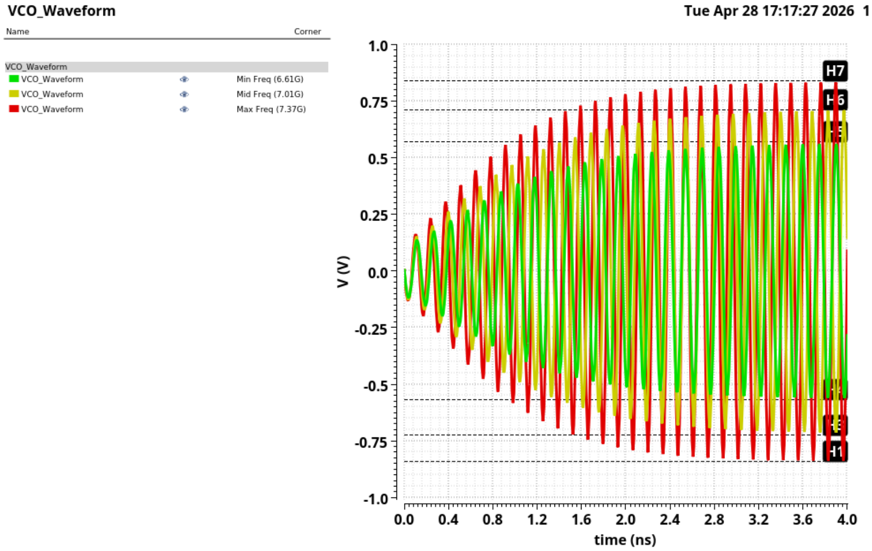


Figure 7: Transient VCO output waveform at the low-, mid-, and high-frequency tuning points. All three cases settle to a differential output swing greater than 1 V_{ppd}.

6.3 VCO Tuning Curve: Oscillation Frequency vs. Control Voltage

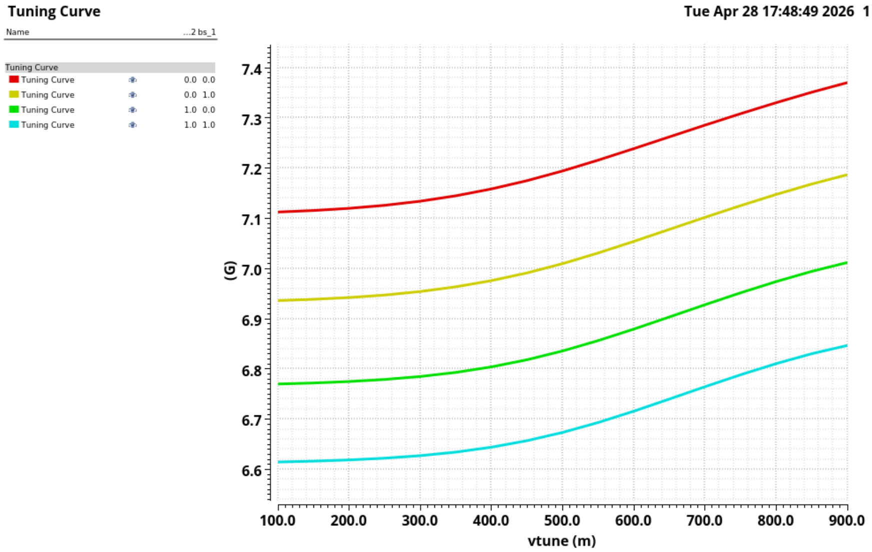


Figure 8: Simulated VCO tuning curves for the four digital band settings. The oscillator covers 6.615–7.370 GHz, with adjacent overlaps from lowest to highest band of 32.5% for B_{11}/B_{10}, 30.8% for B_{10}/B_{01}, and 29.1% for B_{01}/B_{00}.

6.4 VCO Gain K_{VCO} vs. Control Voltage

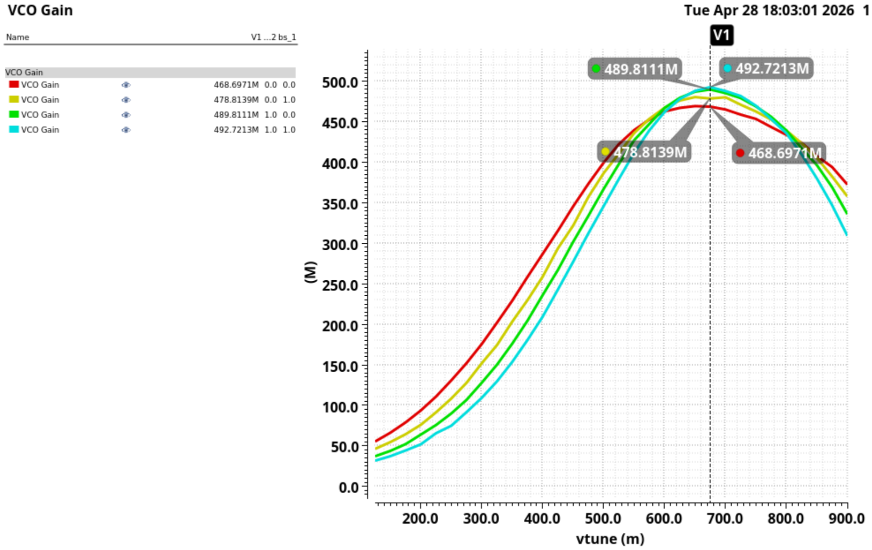


Figure 9: Simulated K_{VCO} versus V_{tune} for all four digital band settings. The maximum K_{VCO} is 492.9 MHz/V, which satisfies the 500 MHz/V specification.

6.5 Phase Noise vs. Offset Frequency at the Low, Mid, and High-Frequency Tuning Points

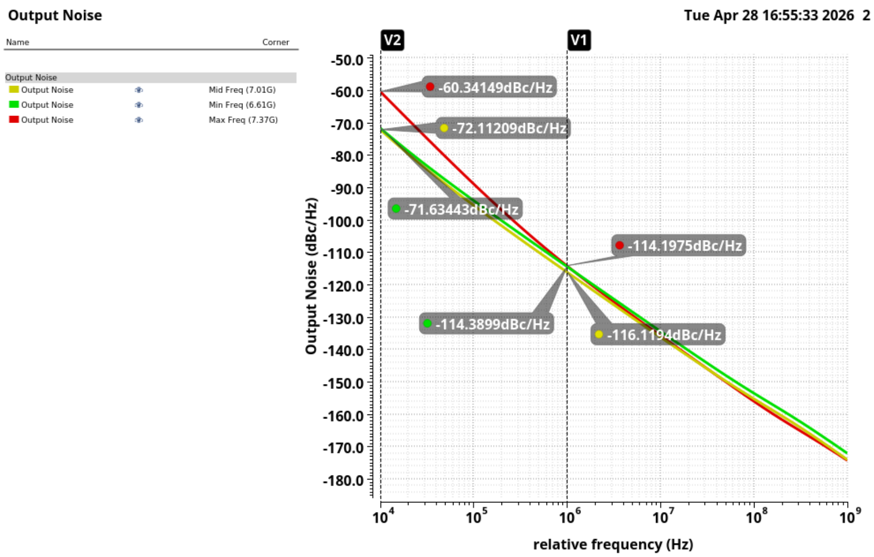


Figure 10: The min-, mid-, and max-frequency phase-noise cases were simulated using $(B_1, B_2, V_{\text{tune}}) = (1, 1, 0.1\text{ V})$, $(1, 0, 0.5\text{ V})$, and $(0, 0, 0.9\text{ V})$, corresponding to 6.61 GHz, 7.01 GHz, and 7.37 GHz, respectively.

6.6 Phase Noise at 1 MHz Offset vs. Control Voltage

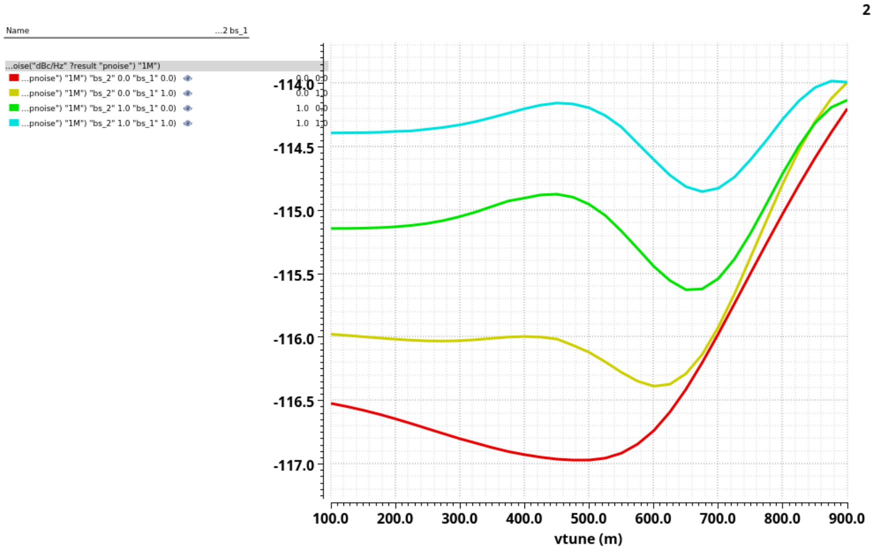


Figure 11: Simulated phase noise at a 1 MHz offset versus V_{tune} for all four digital band settings. The phase noise remains below −114 dBc/Hz across the tuning range.

7 References

- Brian Floyd (Professor): ECE 712 Lecture Notes
- Balram Palli (Teaching Assistant): Advice and Debugging Help During Online Office Hours
- ASITIC's Website Documentation

Appendix

A Voltage Controlled Oscillator Schematics (DC Operating Points)

A.1 Voltage Controlled Oscillator Core

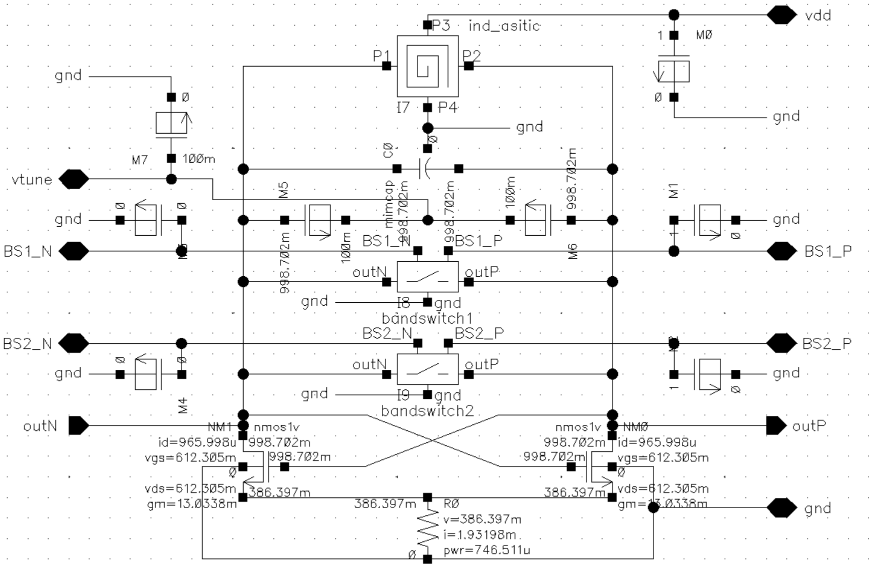


Figure 12

A.2 Voltage Controlled Oscillator Test Bench

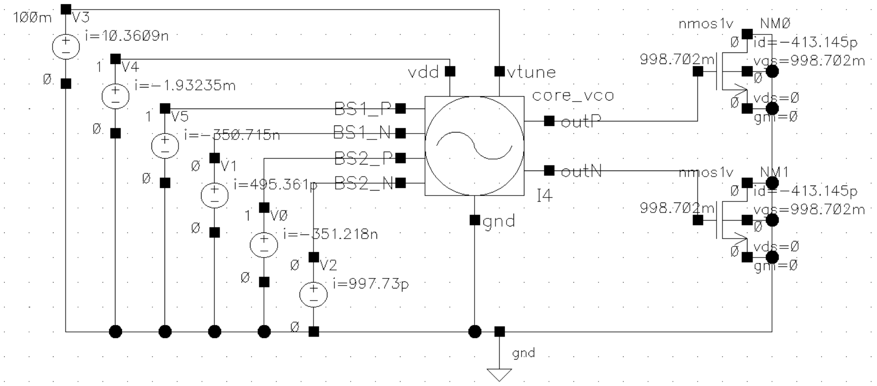
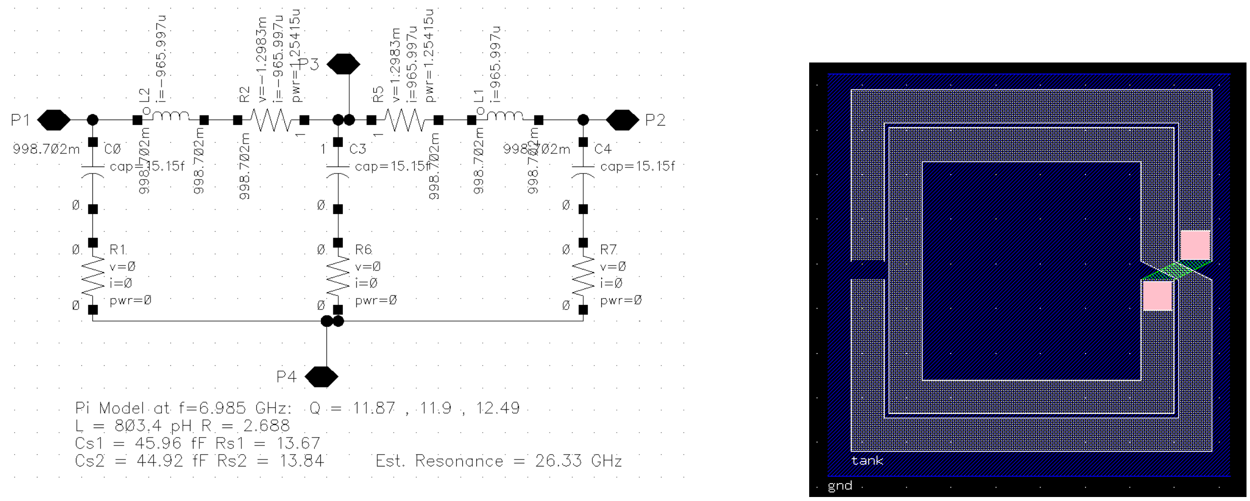


Figure 13

A.3 ASITIC Modeled Tank Inductor

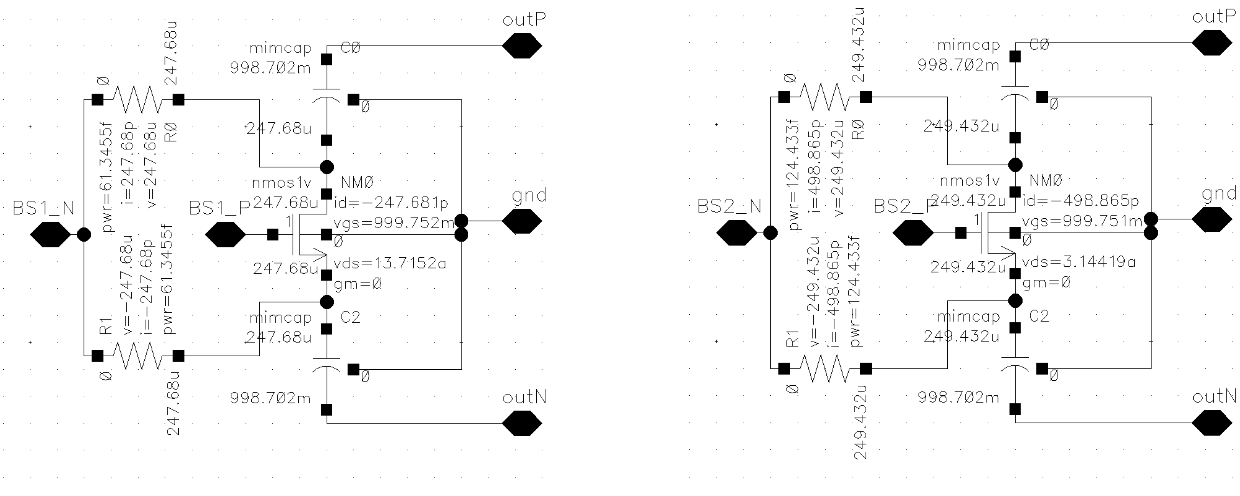


(a) Schematic

(b) Layout

Figure 14

A.4 Digitally Controlled Band Switches



(a) Band Switch 1

(b) Band Switch 2

Figure 15

A.5 Analog Varactor Test Bench

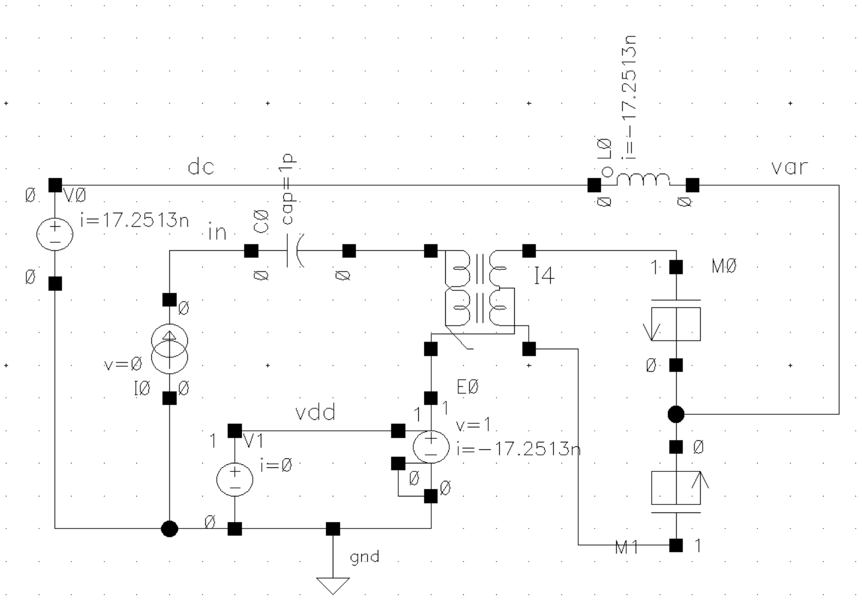
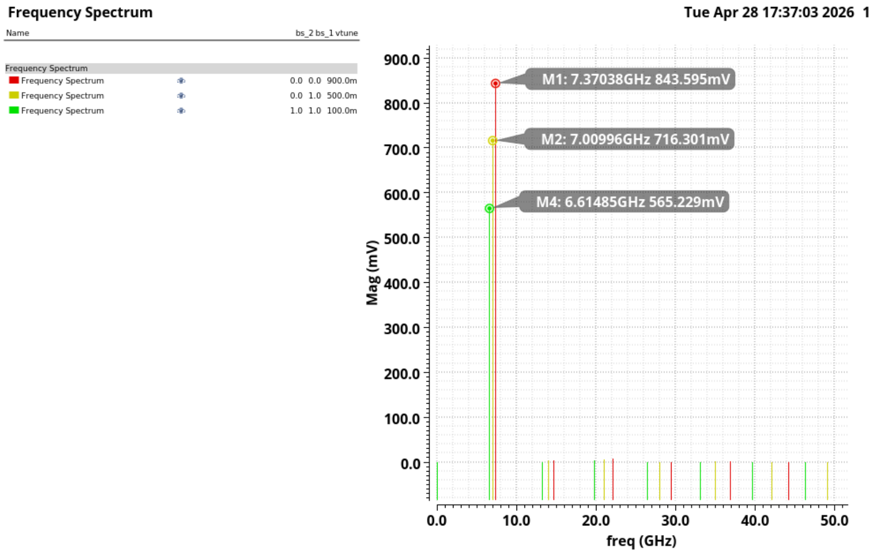


Figure 16

B Extra Simulation Plots

B.1 Frequency Response at the Low, Mid, and High-Frequency Tuning Points



Frequency Spectrum

Tue Apr 28 17:37:03 2026 1

Name	bs_2	bs_1	vtune
Frequency Spectrum			
🟥 Frequency Spectrum	0.0	0.0	900.0m
🟨 Frequency Spectrum	0.0	1.0	500.0m
🟩 Frequency Spectrum	1.0	1.0	100.0m

Figure 17: PSS output spectra at the low-, mid-, and high-frequency tuning points, showing fundamental oscillation frequencies of 6.61 GHz, 7.01 GHz, and 7.37 GHz.

B.2 Fun VCO Period Plot as Vtune is Swept