A Unilateral (Cascode) Source-Degenerated Low-Noise Amplifier with ASITIC Inductors in 45-nm CMOS Technology

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Academic Integrity Statement

I certify that this report represents my original work. No prior-year designs, reports, or external unpublished materials were used. All assistance from tools such as AI is disclosed where applicable.

Contents

Abbreviations List

Acronym	Definition
ASITIC	Analysis of Si Inductors and Transformers for ICs
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
CG	Common-Gate
CS	Common-Source
dB	Decibel
DC	Direct Current
GND	Electrical Ground
IC	Integrated Circuit
LNA	Low-Noise Amplifier
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-Channel Metal-Oxide-Semiconductor
PVT	Process, Voltage, and Temperature
VDD	Positive Supply Voltage

1 Abstract

The Unilateral (Cascode) Source-Degenerated Low-Noise Amplifier was implemented in 45 nm CMOS Technology using the Cadence GPDK045 design kit and ASITIC-based inductor models. The architecture utilizes a common source and common gate NMOS transistor for the cascode and two additional MOSFET's for the biasing. The design was made for the WLAN Channel 207 802.11ax (6.905 to 7.065 GHz) and achieved a 2-dB bandwidth spanning from 5.73 to 7.44 GHz. The results from the simulations showed and in-band noise figure below 1.20dB, center-frequency gain of 18.46 dB, input-referred 1-dB compression point of -14.24 dBm, and input-referred IP3 of -2.99 dBm. The amplifier also achieved the input/output matching, power consumption, and stability requirements, with $P_{DC} = 9.96mW$ and unconditional stability across 10 MHz to 100 GHz. Overall, the design met all specified LNA performance targets. Significant cuts to the S21, S11, and S22 performance were made at the last stage of the design to hit the $P_{DC} < 10mW$ specification.

2 Specifications Table

Summary of performance versus required specifications. Specifications not met appear in red.

Metric	**LNA Specification**	**Achieved Value**	**Meets Spec?**
Frequency range with 2-dB BW > 160 MHz	6905–7065 MHz	5.73–7.44 MHz	Yes
Noise Figure	< 1.7 dB	< 1.20 dB in-band	Yes
Compression Point	$\text{iP}_{1\text{dB}} > -15$ dBm	-14.24 dBm	Yes
Power Metric	Pdc < 10 mW	9.96 mW	Yes
Operating Power Gain	15 dB at center	18.46 dB at center	Yes
$\lvert S_{11}\rvert$ across BW	< -10 dB	< -10.82 dB in-band	Yes
$\lvert S_{22}\rvert$ across BW	< -10 dB	< -10.75 dB in-band	Yes
IP3	10 dB higher than compression	-2.99 dBm	Yes
Stability and Robustness	Unconditional across 10 MHz–100 GHz	$K > 2.46$, $B_1 > 451n$ across 10 MHz–100 GHz	Yes

Table 1: LNA design specifications and achieved performance.

3 Use of AI Tools

OpenAI's ChatGPT 5.4 Model was used for textual grammar edits, help with LATEX formatting, and revisions for clarity in the report.

4 Technical Discussion

4.1 Cascode LNA Architecture Overview

Low-noise amplifiers (LNAs) are used in applications where signal-to-noise ratio is especially important. They are typically used for weak input signals, where the goal is to amplify the signal without adding much noise or distorting it.

Thus it makes sense that a LNA is designed to provide a low noise figure over the required bandwidth (BW) in which it operates, along with moderate gain across that BW. The gain for the amplifier should be high enough to suppresses the noise contribution of later stages electrical component stages (such as mixers, filters, or other power amplifiers) but not too high that it reduces the linearity of those stages. To reduce noise and maximize power transfer, the LNA requires input and output matching over the bandwidth to most commonly 50 Ω. The input of the LNA is often at the beginning of a receiver architecture and can come from an antenna in radio applications. At the output, we then need to output match when the signal is driven-off chip to component with a different impedance. In terms of design needs, the LNA wants to have low power consumption, high linearity, unconditional stability, and robustness across process, voltage, and temperature (PVT).

The design process used here is based on choosing the input impedance Z_{in} to be the complex conjugate of the optimum noise impedance. This allows us to design for maximum signal power transfer into the amplifier while simultaneously creating an impedance that minimizes noise.

To achieve input power matching, inductive degeneration is used as a common-source stage does not provide a real-input impedance that is reasonable for matching. At low frequencies, the gate input impedance is large and is largely independent of the source impedance. However, at higher frequencies, C_{gs} looks like a short, and the source impedance begins affects the input impedance. By adding a source degeneration inductor, a real part is added to the input impedance. This real part is proportional to the source inductance and operating frequency such that we can tune the impedance closed to 50 Ω.

I utilized a cascode to reduce the Miller effect associated with the common-source transistor and for reverse isolation purposes between the input and output stages. In a unilateral amplifier, the signal flow occurs mainly from input to output, this isolates the input and output matching stages (a much easier process of matching when the input and output are done independently). The gate inductor is then used to complete the input match. Because this inductor is directly in the signal path, its Q factor should be as high as possible to avoid increasing the noise figure.

For the output matching network, a drain inductor is used to transform the real impedance seen looking into the output of the cascode stage to 50 Ω. To maximize gain, the drain inductance is increased to a large value. Then a series capacitor is then used to complete the output match.

4.2 Transistor Sizing and Biasing Strategy

My design process began by setting up the cascode amplifier and its current mirror bias network. The NMOS cascode uses a common source input stage follow by a common gate to boost the output impedance and therefore gain. The cascode is especially favorable in the LNA application to isolate the input from the output. For the initial design, I used single-finger MOSFETs with $L = 60\,\text{nm}$ and $W = 1\,\mu\text{m}$ for all four transistors. I then swept the bias current to find the optimum current density. Given the design constraint of a $200\,\mu\text{A}$ current supply, I found that there was little improvement in $NF_{\min}$ for currents above approximately $20\,\mu\text{A}$ after sweeping. The motivation for biasing above the absolute minimum current is to ensure that thermal noise dominates over flicker noise. The operating point was chosen by plotting $NF_{\min}$ versus current density and selecting a current within approximately 1 dB of the minimum value. There was a wide acceptable bias range from $20\,\mu\text{A}$ to $200\,\mu\text{A}$.

Next, I replaced the ideal 1 H inductor in the input bias T with a moderate-value resistor on m1 from the gpdk045 kit, R_{big}. I swept the value of R_{big} and plotted NF, $NF_{\min}$, and S_{11}. There was a relatively broad range, approximately 5 kΩ to 20 kΩ, over which $NF_{\min}$ changed very little. The main criteria for choosing R_{big} was to identify the point at which $NF_{\min}$ was beyond the flicker region, which occurred around 10 kΩ. We want to isolate the cascode from the biasing network with this resistor such that noise cannot move laterally across the circuit to the output and degrade the NF.

I then scaled the transistor finger count until the optimum noise resistance approached approximately 50 Ω. To do this, I plotted the optimum noise reflection coefficient, Γ_{opt}, on a Z-Smith chart together with NF and $NF_{\min}$ on a rectangular graph. The goal was to increase device size until the optimum impedance moved close to the desired input matching region. As the device width increased, Γ_{opt} shifted leftward on the Z-Smith chart, corresponding to a smaller real optimum impedance. This trend is expected because increasing device size lowers the total resistance (a parallel network). The finger count was chosen such that the optimum noise impedance moved close to the 50 Ω region while maintaining good noise performance. I settled on 337 fingers (and later moved to a multiplier of 84 with 4 fingers for pss convergence simulation reasons) for the common-source and common-gate of the cascode. For simplicity of the design, I did not differ the number of fingers for the common-source and common-gate nor use multipliers in the initial stages before the linearity simulations.

4.3 Inductor Modeling and ASITIC

In terms of inductor modeling and ASITIC, this part of the project definitely took the longest to set up. A lot of the work came down to managing parasitics and going back and forth between Cadence and ASITIC.

Next, I added a source degeneration inductor to create a real input impedance close to 50 Ω. I started with an ideal inductor and was able to get the input match working very easily. After that, I switched to an `indQ` component with reasonable Q values, roughly in the 4–12 range. I swept the source inductor until I got a real impedance that was worth matching to. The source inductor value was chosen so that, together with the gate inductor and its parasitics, the overall series inductance would move S_{11} near the center of the Z-Smith chart over the in-band frequencies. Because of that, the source inductor value was developed in parallel with the ASITIC models. As the source inductor did not lye directly in the RF signal path, its Q factor did not have the largest importance in terms of its contribution to NF.

Since there was no restrictions regarding layout constraint for this design (I can make the inductors as large as I want), I found that using fewer turns with large inductors helped a lot with improving the ASITIC-predicted inductor Q. I also found that making the inner hole dimensions about the same as the metal width, while using minimum spacing of 1 μm, gave better results. For the source inductor, I ended up using a 1-turn spiral on metal layer `m6`, which gave a Q of about 9.5. I then iterated on that design using both ASITIC and Cadence sweeps of the `indQ` component until the impedance landed slightly before the 50 Ω line on the Z-Smith chart. I found that landing the impedance before the 50 Ω line proved to be easier to be easier to match to 50 Ω with the associated series resistance parasitic for the gate inductor.

Then I added the gate inductor and swept `indQ` values with Q around 10 while tuning the inductance until the series inductor moved S_{11} close to the center of the Z-Smith chart. I followed the same basic process here: sweep the inductor values in Cadence, estimate the Q and inductance I wanted, and then design a matching inductor in ASITIC. For the gate inductor, I ended up with a 2.5-turn spiral and adjusted the inner hole dimensions and metal width, again with minimum 1 μm spacing, until I got the inductance I needed with a Q of about 12. I also added a ground shield on the `m1` layer to improve the performance even further. The ground shield serves to reduce the parasitics between the substrate and inductor and therefore boost the Q value. The more iteration in this step, resulted in higher Q values and directly improved the NF.

For the drain inductor, I used the same general approach. I first swept the `indQ` value in Cadence to figure out the inductance I needed, then designed the corresponding inductor in ASITIC. This inductor also used 2.5 turns with minimum spacing, and I adjusted the inner hole dimensions and metal width until I got the required inductance with a Q of about 11.5. For the drain inductor, I designed my ASITIC inductor for the highest value that was reasonable after sweeping such that I would increase my output impedance and max gain.

After simulating the output impedance, I designed the matching network by adding a series capacitor to complete the output match. This value was chosen by sweeping the capacitor value until the S22 value landed near the center of the Z-Smith Chart. The design process with real inductors and associated parasitics was very much a non-linear design process with lots of iteration involved.

Before finishing the matching, I gradually replaced the ideal components with more realistic GPDK045 models. I used the non-ideal `mimcap` component for the output match, the `resm1` component for the resistor, and the `nmoscap1v` component for the input AC coupling capacitor. After inserting these components, I observed slight shifts in the matching conditions, but nothing too severe.

4.4 Linearity Optimization

To improve the linearity of the circuit, I first tried increasing the current reference. That helped somewhat, but it mainly came with the downside of much higher power consumption. I also increased V_{DD} to improve the 1 dB compression point. Along with slightly reducing the number of fingers, these changes pushed the 1 dB compression point above -15 dBm and got the IP3 to more than 10 dB above that value. However, at that stage the design had around 340 fingers, a 2.5 V supply, and an i_{ref} of 120 μA, and when I checked the DC power consumption, it was nearly 100 mW, about 10 times higher than the project specification.

To bring the power back down without redesigning the gate, source, and drain inductors, I had to give up some of the matching and gain. My earlier design had very strong matching, around -25 dB for both S_{11} and S_{22}, but after reducing the bias and supply voltage, those values moved closer to about -11 dB. The gain also dropped from about 23 dB to about 18 dB. I found that I needed to lower V_{DD} to 1.34 V and reduce the current reference to 18 μA in order to get the total DC power below the 10 mW limit while still using the large transistor size. Changing the biasing did disturb the input match, but the design was still able to meet the project specs.

Throughout this process, I also kept an eye on the noise figure and the K and B_1 stability metrics as I lowered the reference current into a region where flicker noise started to become more noticeable. At a current reference of around 80 μA, the noise figure was approximately 1 dB, but it increased by about 0.4 dB when I reduced the current reference to 18 μA. I also found that lowering the current much below 18 μA caused the circuit stability to degrade.

5 Low-Noise Amplifier Schematics (Design Values)

5.1 Low-Noise Amplifier Core

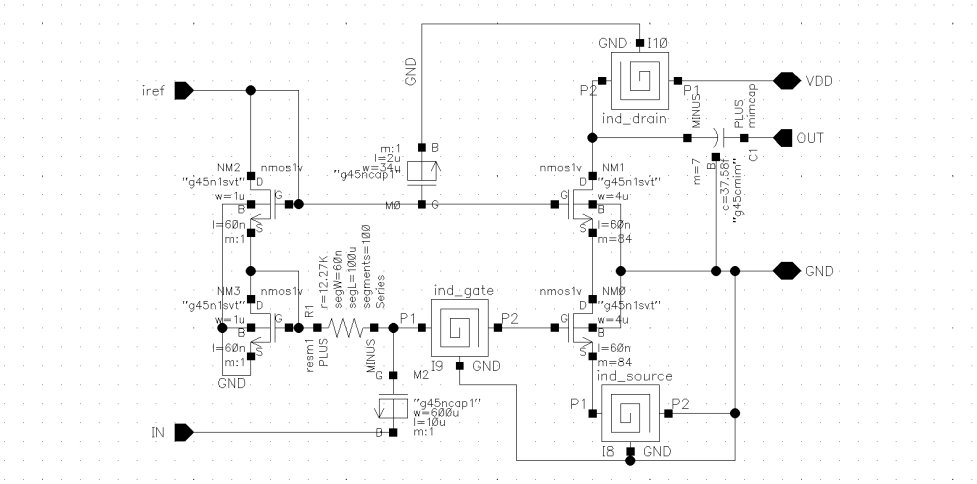


Figure 1: The LNA core featuring the three custom inductors, four MOSFETS's, an AC coupling capacitor, a matching capacitor, and a resistor. All components were from the gpdk045 library.

5.2 Low-Noise Amplifier Test Bench

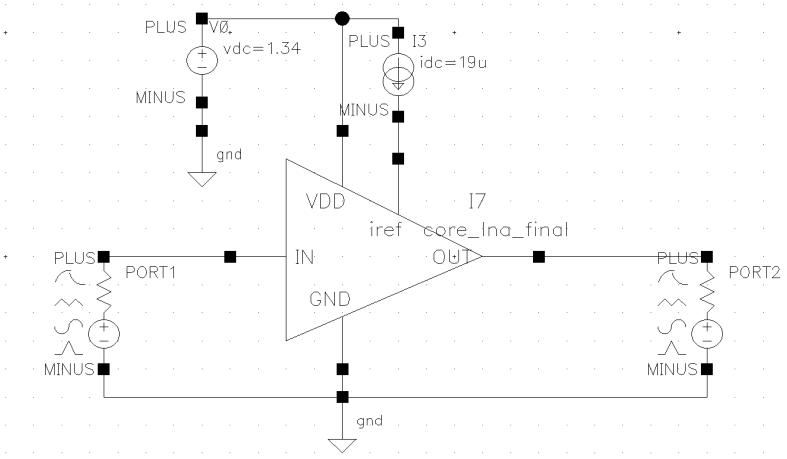
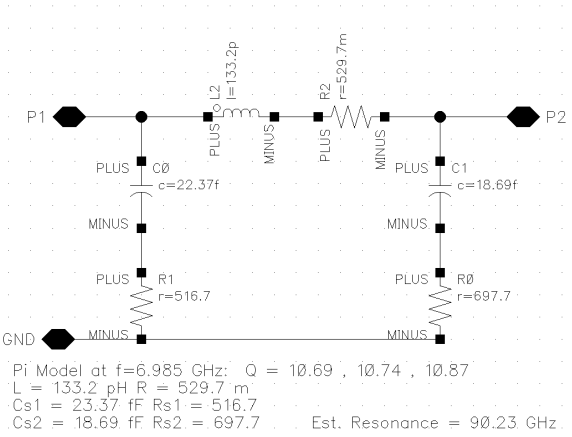
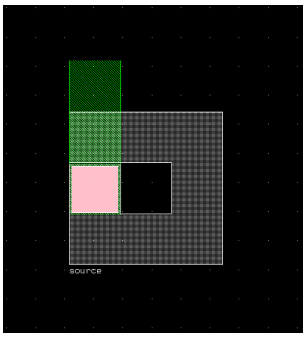


Figure 2: The LNA test bench uses an ideal 19 μA current source for biasing, an ideal V_{DD} supply of 1.34 V, and 50 Ω input and output ports.

5.3 ASITIC Modeled Source Inductor



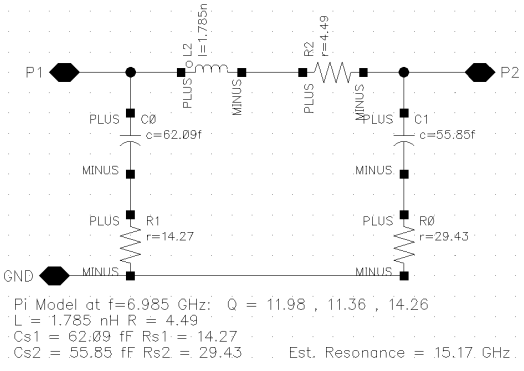
(a) Schematic



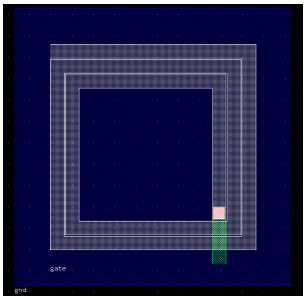
(b) Layout

Figure 3: ASITIC-modeled source inductor schematic and layout. The inductor was generated with an inner hole dimension of 35 μm, metal width of 35 μm, spacing of 1 μm, one turn, top metal layer `m6`, and an exit segment on `m5`.

5.4 ASITIC Modeled Gate Inductor



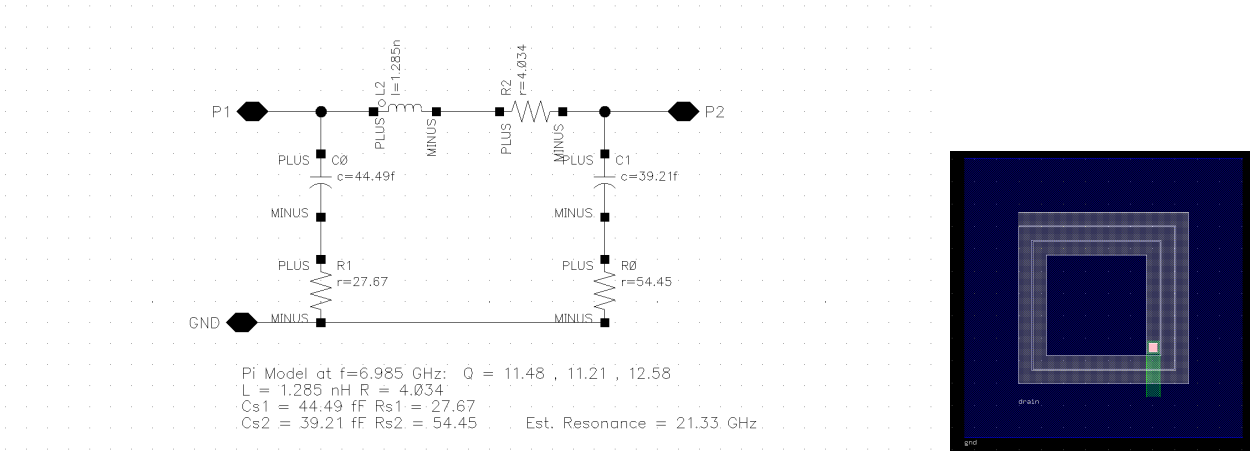
(a) Schematic



(b) Layout

Figure 4: ASITIC-modeled gate inductor schematic and layout. The inductor was generated with an inner hole dimension of 125 μm, metal width of 13 μm, spacing of 1 μm, 2.5 turns, top metal layer `m6`, and an exit segment on `m5`. A ground shield was also included using metal layer `m1` with dimensions of 260 μm by 260 μm, electrical phase +1, centered at the chip origin, and oriented at 0°.

5.5 ASITIC Modeled Drain Inductor



(a) Schematic (b) Layout

Figure 5: ASITIC-modeled drain inductor schematic and layout. The inductor was generated with an inner hole dimension of 90 μm, metal width of 12 μm, spacing of 1 μm, 2.5 turns, top metal layer `m6`, and an exit segment on `m5`. A ground shield was also included using metal layer `m1` with dimensions of 250 μm by 250 μm, electrical phase +1, centered at the chip origin, and oriented at 0°.

6 Low-Noise Amplifier Simulation Results

6.1 Operating Power Gain and $G_{\max}$ vs. Frequency

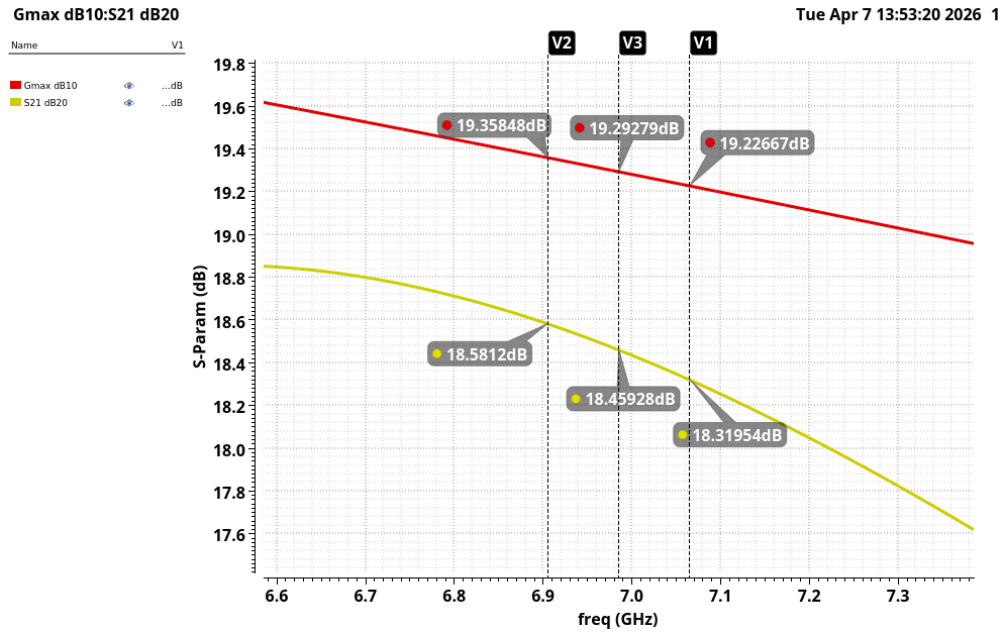


Figure 6: The LNA achieves about 18.46 dB gain at center frequency.

6.2 Noise Figure NF and Minimum Noise Figure $NF_{\min}$ vs. Frequency

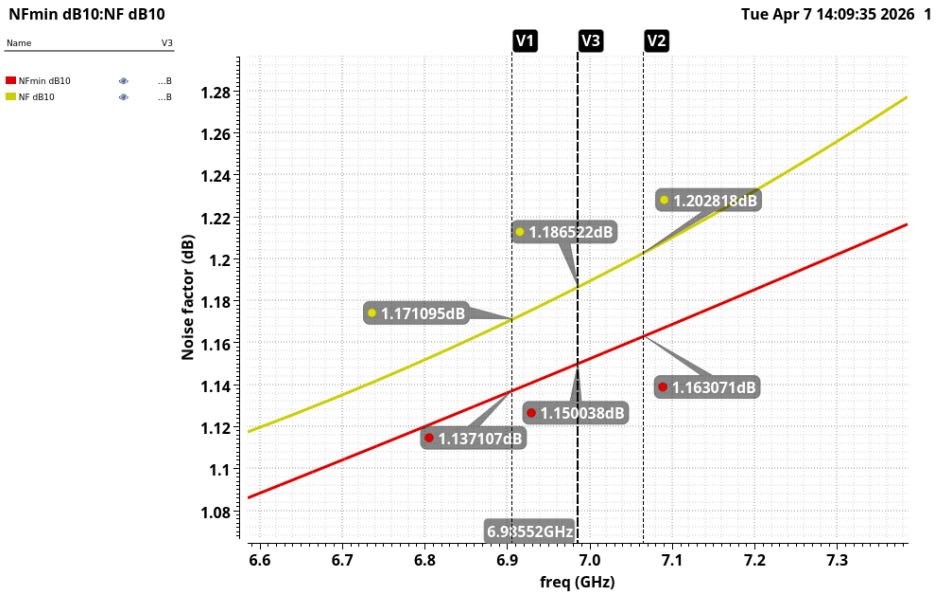


Figure 7: Simulated NF and $NF_{\min}$ versus frequency. The in-band noise figure remains below 1.20 dB, satisfying the $NF < 1.7$ dB requirement.

6.3 Log-Magnitude of S_{11} and S_{22} vs. Frequency

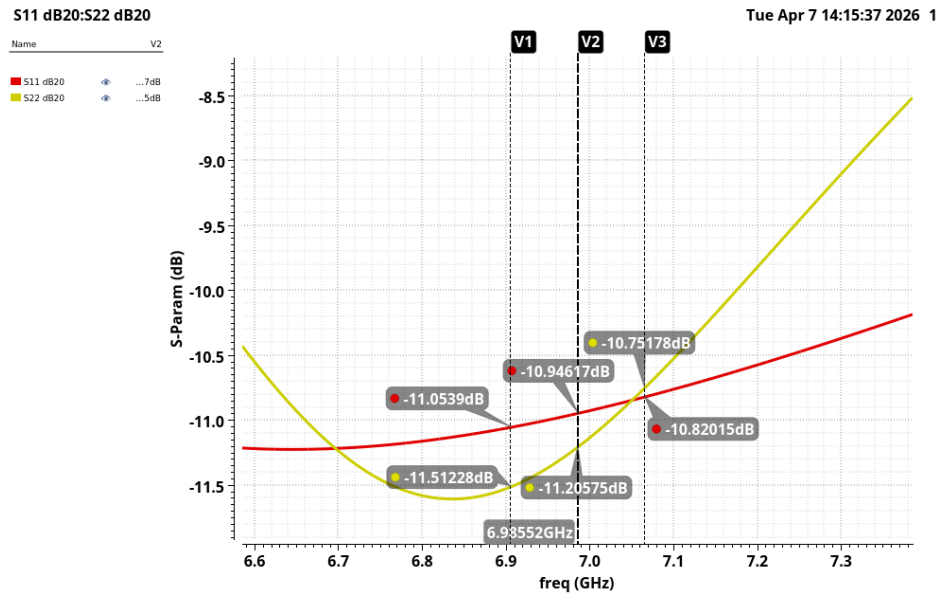


Figure 8: Both input and output return losses remain below $-10\,\mathrm{dB}$ across the operating band.

6.4 S_{11}, S_{22}, and Γ_{opt} on the Smith Chart

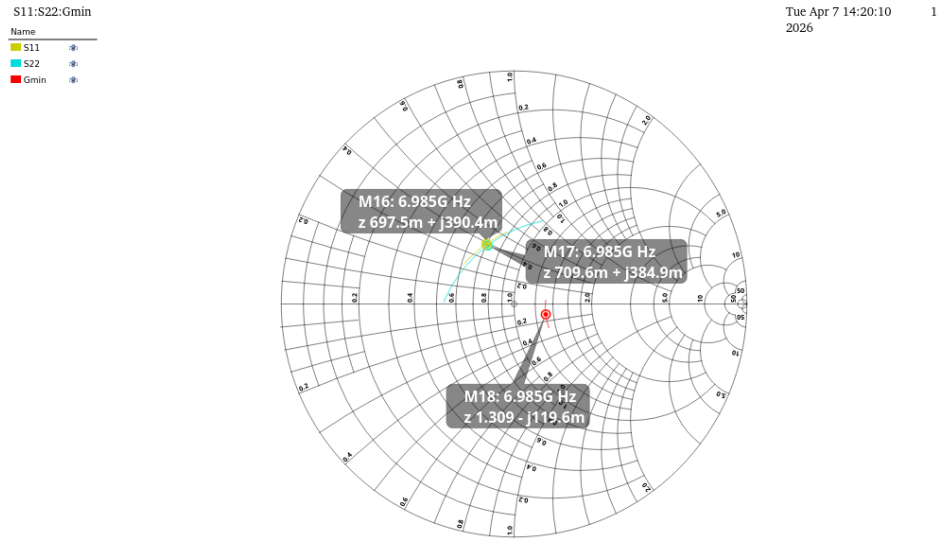


Figure 9: Smith chart of S_{11}, S_{22}, and Γ_{opt} near the center frequency. Interestingly enough, the S11 and S22 are almost right on top of each other.

6.5 $P_{1\mathrm{dB}}$ from Swept Power Plot: P_{out} vs. P_{in}

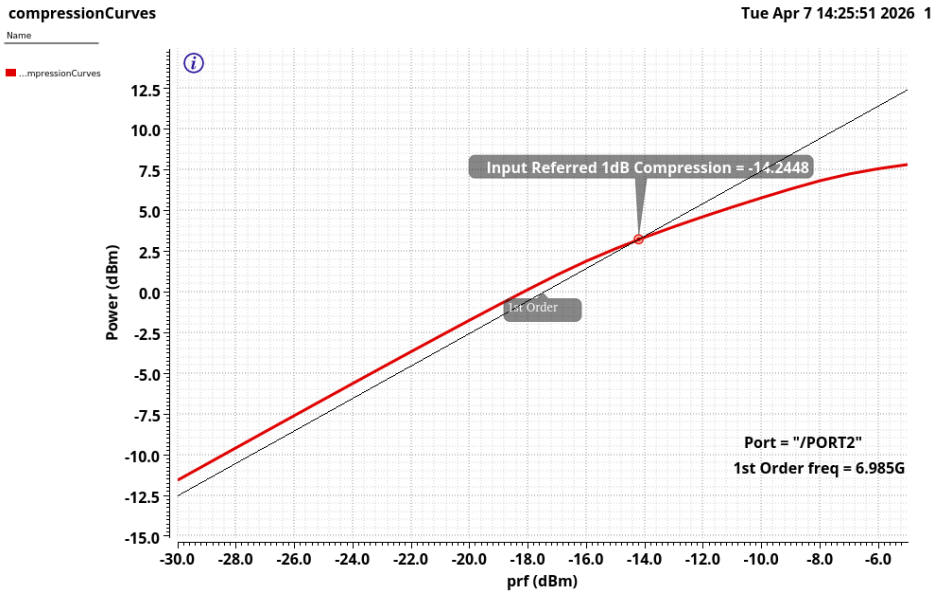


Figure 10: Swept-power compression plot used to extract the input-referred 1-dB compression point, giving $iP_{1\mathrm{dB}} \approx -14.24\,\mathrm{dBm}$.

6.6 IP3 from Swept Power Plot: P_{out} and IM3 vs. P_{in}

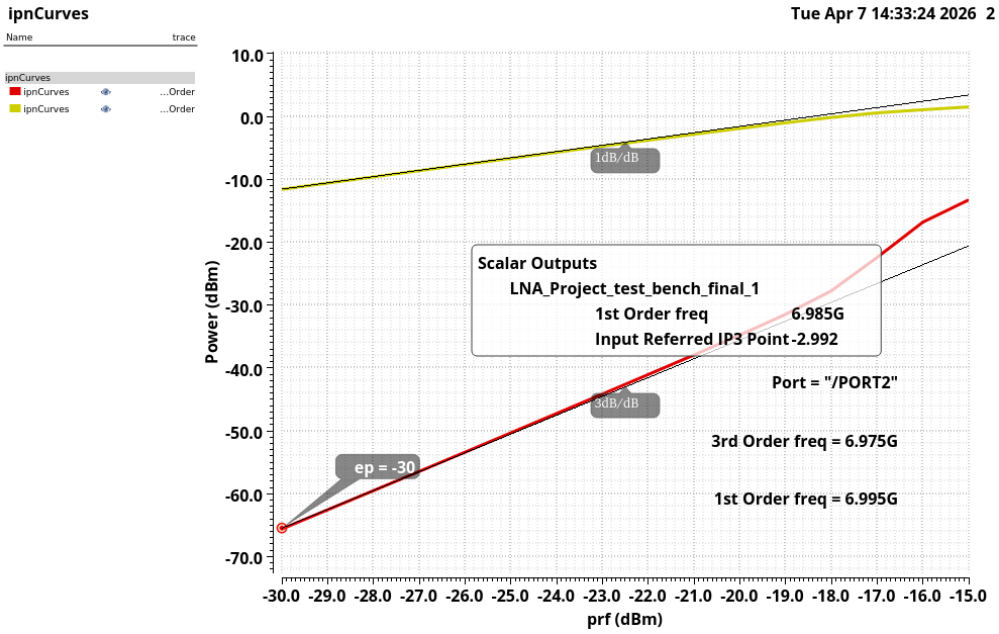


Figure 11: Swept-power IP3 plot of the output fundamental and IM3 product versus input power, yielding an input-referred IP3 of about $-2.99\,\mathrm{dBm}$.

6.7 DC-Operating Point Power Consumption

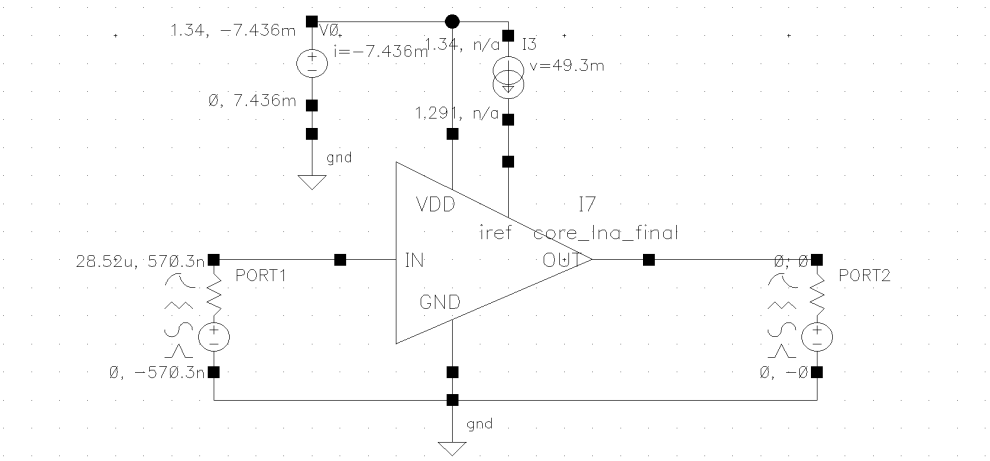


Figure 12: DC operating point of the LNA test bench used to calculate power consumption, which is approximately 9.96 mW.

6.8 Stability Factors K and B_1 vs. Frequency

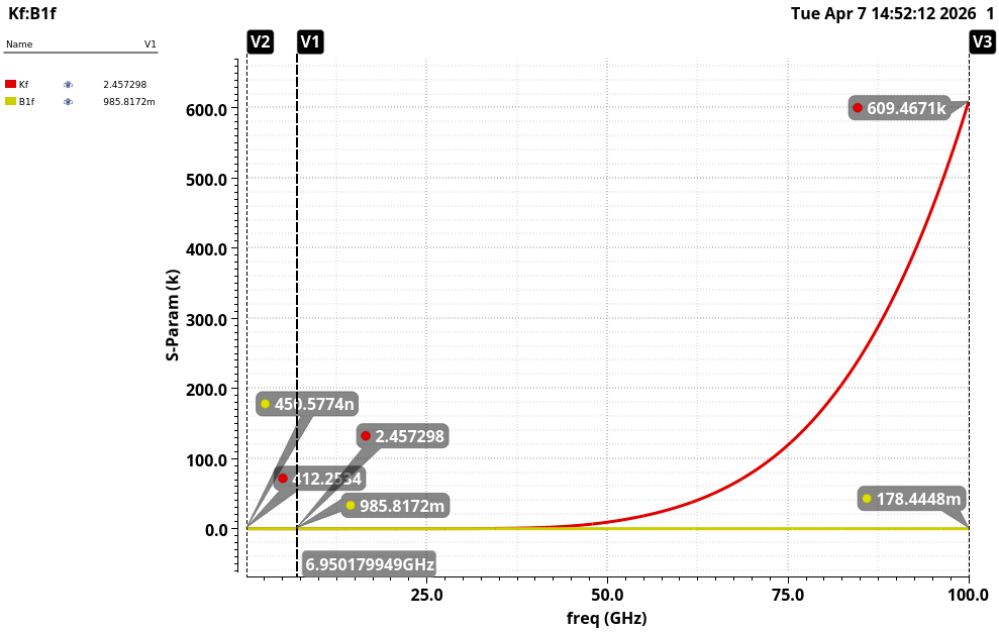


Figure 13: Stability factors K and B_1 versus frequency from 10 MHz to 100 GHz, confirming unconditional stability over the full range.

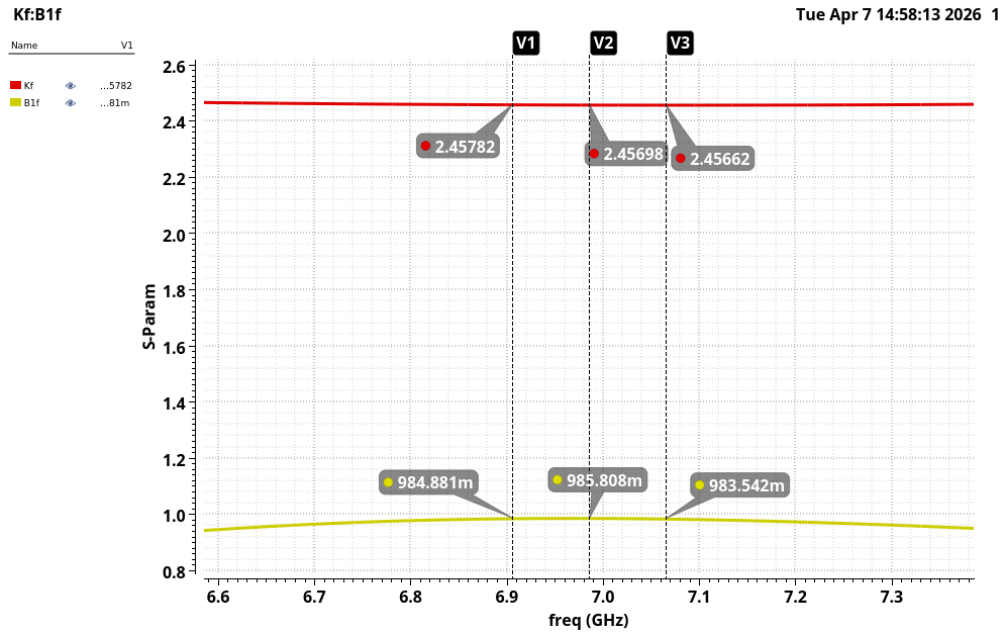


Figure 14: Expanded view of K and B_1 across the operating band, showing stable in-band operation with $K > 1$ and $B_1 > 0$.

7 Discussion

I think the key to this project was intelligent sweeping. In the presence of parasitics, knowing whether you need more inductance or less inductance is very important because of how those parasitics shift the S-parameters on the Smith chart. Before starting the project, I made sure to really understand the fundamentals. That was something I do not think I did well enough on the 511 amplifier. Having that foundation helped me move through this design much more intelligently without relying on guesswork, and the overall process felt much more methodical.

For the inductors, I think using the `indq` components before designing the actual inductors in ASITIC worked well. That let me estimate the rough inductance values I needed and also see how different Q values moved the impedance around the Smith chart. For a while, I tried building my own parasitic inductor model with equations for the shunt resistances, shunt capacitances, and series resistance based on Q and resonance, but it ended up being too difficult to match reliably to the ASITIC results. Because of that, I went back to using the `indq` models as a starting point. What I ended up doing was choosing an inductance value, sweeping it, designing that value in ASITIC, plugging it into the circuit, disabling the `indq` version, and then checking where the design landed on the Smith chart. I repeated that process several times for the different inductors.

A few strategies worked well for improving inductor Q in ASITIC. In general, thicker metal widths and smaller spacing helped. For the source inductor, I used only a single turn and found it difficult to get the Q much above 10 because the inductance value was so small, around 100 pH. For the gate and drain inductors, I used 2.5 turns and values in roughly the 1–2 nH range, where it was much easier to achieve a higher Q. I also found that the input and exit segments in ASITIC introduced additional series resistance, which had a more noticeable effect for the smaller inductance values. Keeping the number of turns relatively low also helped improve Q and reduce parasitics.

One mistake I made early on was not paying enough attention to power consumption. I settled on 337 fingers while sweeping the $G_{\min}$ parameter and was using a standard 1.8 V supply with an i_{ref} of about 90 μA to stay out of the flicker-noise region. At that stage, I did not realize the circuit was consuming nearly 100 mW of power. It was only after I had finished the input matching, with more than 20 dB of gain and both S_{11} and S_{22} below -20 dB, that I realized the power consumption was far too high. I found that I could reduce the power significantly by lowering the supply voltage to around 1.3 V and reducing i_{ref} to around 20 μA. The final design does not show the same level of input and output matching because of that late-stage adjustment to the circuit biasing and headroom, but it still surprisingly meets the matching requirements.

I understand now why designing an LNA truly is a game of optimization where you trying to balance noise, power gain, linearity, matching, working over PVT, and power consumption. It is one of those things where until you actually build one, it is very hard to understand the strings attached to the design tradeoffs.

8 Conclusion

Overall, the LNA project was a very important learning experience. It was a great introduction to how important parasitics are in RF design. After going through the LNA design process both with and without parasitics, it became very clear how much easier the design is with ideal components. Once non-ideal Q factors are introduced, the design becomes much more dependent on carefully watching where the reflection coefficients land on the Smith chart and deciding whether the circuit needs more series C, series L, series R, shunt C, shunt L, or shunt R.

One part of the process that felt pretty tedious was moving data back and forth between ASITIC and Cadence. It is honestly surprising that Cadence does not already have a more integrated and reliable mainstream tool for this built directly into Virtuoso. If something like that existed, it would be much easier to achieve better input matches simply because so much less time would be spent on setting up the models and transferring them.

It also felt really good to come away with a solid result on a Cadence project, especially after my team's incomplete 511 amplifier.

9 References

- Brian Floyd (Professor): ECE 712 Lecture Notes
- Balram Palli (Teaching Assistant): Advice and Debugging Help During Online Office Hours
- ASITIC's Website Documentation

Appendix

A Noise Figure and S-Parameter Bandpass Response

A.1 Log-Magnitude of S_{11}, S_{22}, S_{21}, NF, $NF_{\min}$, and $G_{\max}$ vs. Frequency

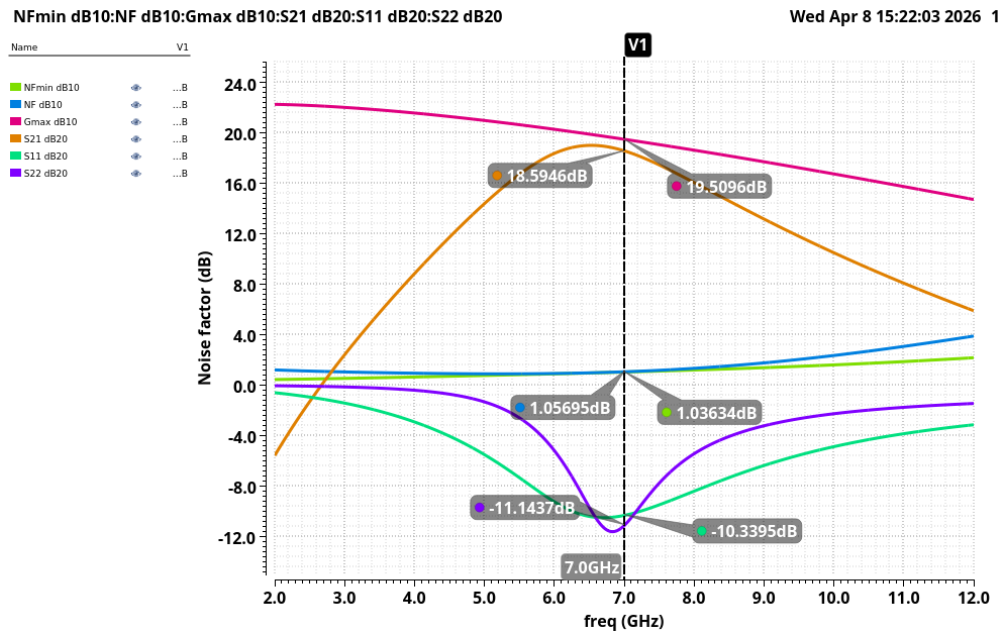


Figure 15: Bandpass nature of the LNA that attenuates/amplifies a specific range of frequencies

B Low-Noise Amplifier Schematics (Operating Points)

B.1 Low-Noise Amplifier Core

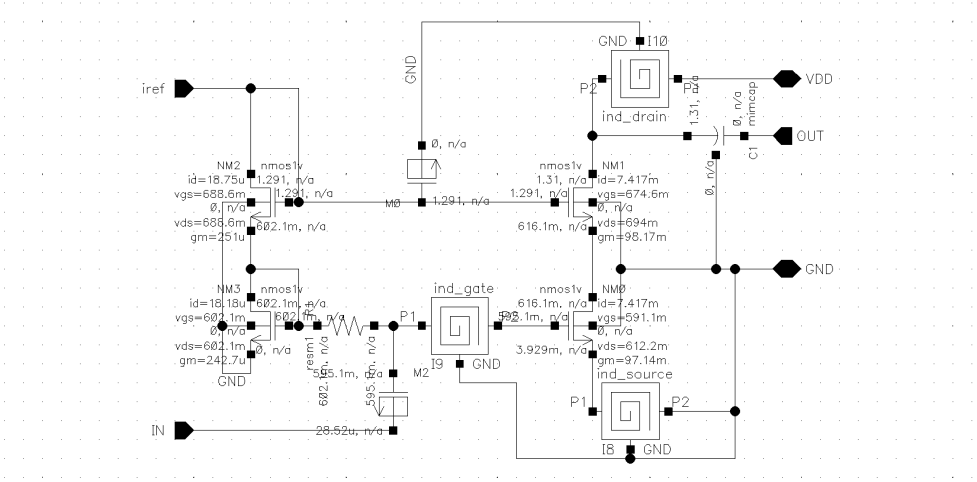


Figure 16: LNA Core DC Operating Points

B.2 Low-Noise Amplifier Test Bench

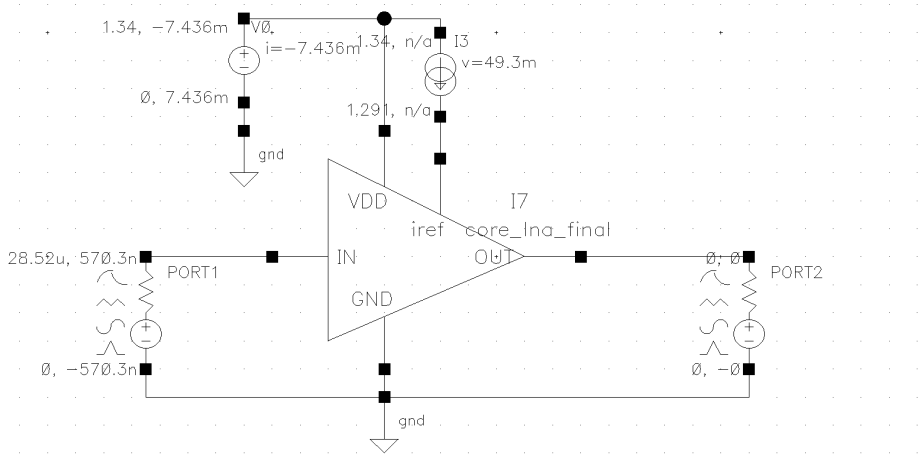
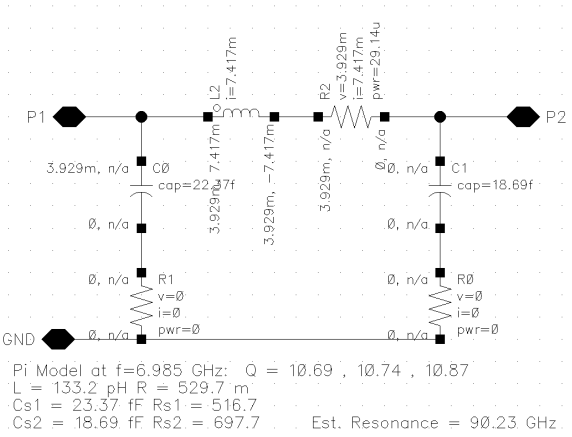
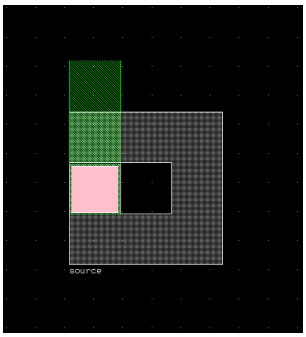


Figure 17: LNA Test Bench DC Operating Points

B.3 ASITIC Modeled Source Inductor



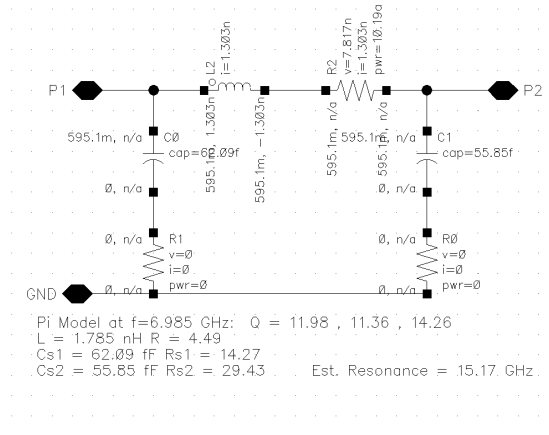
(a) Schematic



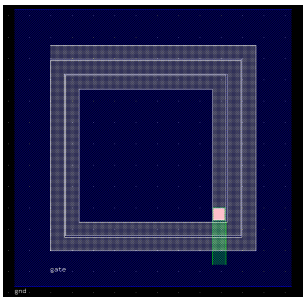
(b) Layout

Figure 18: Source Inductor DC Operating Points

B.4 ASITIC Modeled Gate Inductor



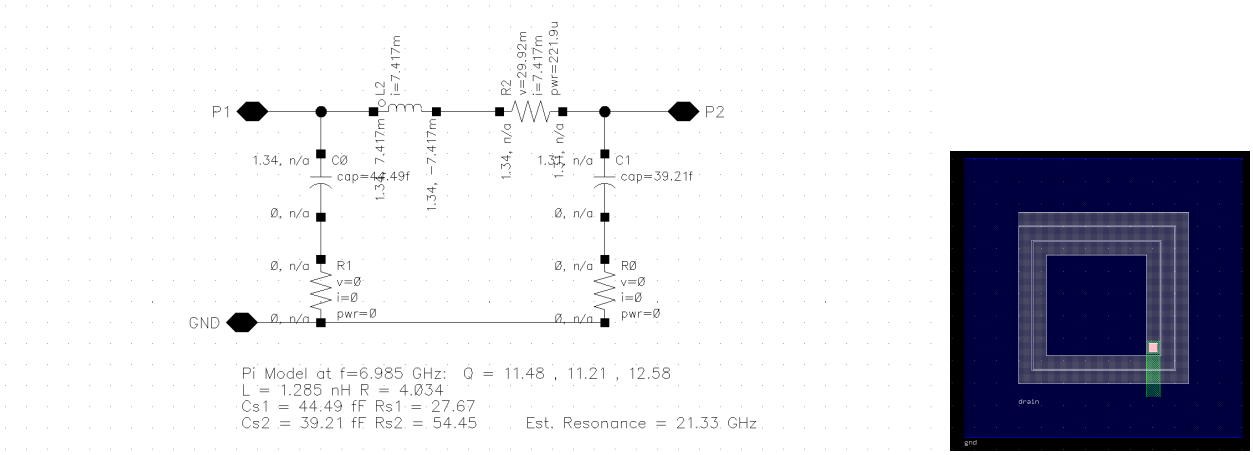
(a) Schematic



(b) Layout

Figure 19: Gate Inductor DC Operating Points

B.5 ASITIC Modeled Drain Inductor



(a) Schematic (b) Layout

Figure 20: Drain Inductor DC Operating Points